Remarks

Claims 23-25, 27-31, 34, and 35 are currently pending in this application. Claims 34 and 35 replace canceled claims 32 and 33.

The Office Action rejected claims 23-25 and 27-29 under 35 U.S.C. § 103(a) as being unpatentable over Deleonibus (U.S. Patent No. 6,091,076) in view of Koh (U.S. Patent No. 6,049,110); rejected claims 23-25 and 27-31 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi et al. (U.S. Patent No. 5,341,028) in view of Imai (U.S. Patent No. 6,297,529) and Koh; rejected claim 32 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi et al. in view of Gardner et al. (U.S. Patent No. 6,096,615) and Koh; rejected claim 33 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi et al. in view of Gardner et al. and Koh, and further in view of Imai; rejected claim 32 under 35 U.S.C. § 103(a) as being unpatentable over Deleonibus in view of Gardner et al. and Koh; and rejected claim 33 under 35 U.S.C. § 103(a) as being unpatentable over Deleonibus in view of Gardner et al. and Koh, and further in view of Imai.

The present invention recited in, for example, claim 23, and claims 24, 25, and 27-31 at least by virtue of dependence, comprises a combination of elements, including: spacers formed on sidewalls of the gate conductor and on the semiconductor layer; extension regions arranged in the semiconductor layer on both sides of the gate conductor and extending under and contacting the spacers and a portion of the gate conductor, wherein a portion of at least one of the extension regions is exposed at a surface of the semiconductor layer by removing at least a part of one of the spacers; and a metal layer formed at least in the exposed portion of the extension region. Similarly, the present invention recited in claim 34, and claim 35 at least by virtue of dependence, comprises a combination of elements, including: first and second sidewall spacers; extension regions provided

under and contacting the first and second sidewall spacers, the extension regions contacting a gate

and extending further under the gate than the source and drain diffusion regions, wherein a portion of

at least one of the extension regions is exposed at a surface of the body region by removing at least a

part of one of the first and second sidewall spacers; and a conductor formed at least in the exposed

portion of the extension region.

In contrast, none of the prior art references applied against the present application discloses or

suggests the combination of elements recited in claims 23-25 and 27-31, including: spacers formed

on sidewalls of the gate conductor and on the semiconductor layer; extension regions arranged in the

semiconductor layer on both sides of the gate conductor and extending under and contacting the

spacers and a portion of the gate conductor, wherein a portion of at least one of the extension regions

is exposed at a surface of the semiconductor layer by removing at least a part of one of the spacers;

and a metal layer formed at least in the exposed portion of the extension region. Further in contrast,

none of the prior art references discloses or suggests the combination of elements recited in claims

34 and 35, including: first and second sidewall spacers; extension regions provided under and

contacting the first and second sidewall spacers, the extension regions contacting a gate and

extending further under the gate than the source and drain diffusion regions, wherein a portion of at

least one of the extension regions is exposed at a surface of the body region by removing at least a

part of one of the first and second sidewall spacers; and a conductor formed at least in the exposed

portion of the extension region.

In light of the above, Applicants submit that none of the prior art references applied against

this application, whether taken alone or in any reasonable combination, discloses or suggests the

combination of elements recited in claims 23-25, 27-31, 34, and 35. Thus, these claims are

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allowable over these references. Applicants, therefore, respectfully request the reconsideration and

withdrawal of the Section 103(a) rejections of these claims.

Applicants respectfully request that this Amendment under 37 C.F.R. § 1.116 be entered,

placing claims 23-25, 27-31, 34, and 35 in condition for allowance. Applicants submit that the

proposed amendments of the claims do not raise new issues or necessitate the undertaking of any

additional search of the art, since all of the elements and their relationships claimed were either

earlier claimed or inherent in the claims as examined. Therefore, this Amendment should allow for

immediate action.

Furthermore, Applicants respectfully point out that the final action presented some new

arguments as to the application of the art against Applicants' invention. It is respectfully submitted

that the entering of the Amendment would allow the Applicants to reply to the final rejections and

place the application in condition for allowance.

Finally, Applicants submit that the entry of the Amendment would place the application in

better form for appeal, should the patentability of the pending claims be disputed.

In view of the foregoing remarks, Applicants request the entry of this Amendment, the

reconsideration of the application, and the timely allowance of the pending claims.

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If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 03-2775. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

CONNOLLY BOVE LODGE & HUTZ LLP

Dated: July 16, 2004

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